UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,064	02/12/2002	Antonio Asaro	00100.00.0130	6702

23418 7590 07/26/2007
VEDDER PRICE KAUFMAN & KAMMHOLZ
222 N. LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
07/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/074,064	ASARO ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31 and 33-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28 and 33-35* is/are rejected.

7)☒ Claim(s) *29-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 28 and 34 have been considered but are moot in view of the new ground(s) of rejection. The examiner notes claim language "forming a register". The examiner had previously interpreted "forming a register" as writing to a register instead of configuring the register. However in light of the specification (particularly figure 3 and accompanying description) and applicants argument the examiner will hereby interpret "forming a register" as configuring a register. Also in accordance with the specification the registers are not to be taken as manufacturing a register.

In regards to applicants argument that claim 10 is allowable for at least similar reasons as claim 1. For example, the reference do not teach or suggest forming configurable registers as claimed: Claim 1 in no way can be interpreted as claiming forming a configurable register.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4-9, 19, 22-23, 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie et al PN 5,859,987 in view of Surugucchi et al PN 6,094,699 and Venkat PN 5,857,083.

In regards to claims 1, 8, 19: Gillespie et al teaches a data bridge system, comprising: an interface (interface to primary PCI bus 9 or alternatively interface to local memory bus 11) for transferring data; a plurality of application-specific integrated circuits (ASICs) (21 and 23); a data bridge operatively coupled to each of the interface and the plurality of ASICs (7). Gillespie et al also teaches the bridge accessing a ROM storing configuration (31 Column 1 lines 59-65). Gillespie et al does not expressly teach the data bridge read only memory storing at least initial values and mask values for each ASIC of the plurality of ASICS. The examiner notes Gillespie et al does teach the bridge having a plurality of Base address registers in accordance with the AGP and PCI specifications, which would inherently need to be configured. Surugucchi et al teaches a bridge (210 or alternatively 210 and 212 taken together) including a mask register storing mask values for masking Base address registers in accordance with the attached peripherals. It would have been obvious to store the configuration mask values in the data bridge ROM of Gillespie et al because this would have consolidated configuration. Venkat teaches storing the initial base addresses in the configuration space of the devices. It would have been obvious to store the initial values in the configuration space of the combination of Gillespie et al in view of Surugucchi et al because this would have consolidated necessary configuration data.

In regards to claims 4, 22: Gillespie et al teaches the bridge having Base address registers. (part of the PCI specification incorporated in Gillespie)

In regards to claims 5-6, 23, 26: Gillespie et al teaches multiple base address registers in accordance with the PCI specification incorporated by reference in Gillespie et al. The PCI specification notes the number of Base address registers in a bus bridge is 6.

In regards to claims 7, 25: Gillespie et al teaches multiple base address registers in accordance with the PCI specification which teaches the base address registers having prefetchable and non-prefetchable and I/O space and non I/O space determinations. PCI spécification page 196.

In regards to claim 9: Gillespie et al teaches a configuration EEPROM. Which is an electrically erasable programmable ROM.

In regards to claim 27: Gillespie et al does not teach the EEPROM being removable. MPEP 2144.04 V C states to make separable is not a patentable distinction.

4. Claims 2-3, 20-21, 24, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie et al PN 5,859,987 in view of Surugucchi et al PN 6,094,699 and Venkat PN 5,857,083 as applied to claim 1 above, and further in view of Applicants admitted prior art.

In regards to claims 2, 20, 24, 33: Gillespie et al does not teach the ASICs being graphics processors. Applicants admitted prior art teaches graphics processors (1020) attaches to a bus. It

would have been obvious to include graphics processors because this would have allowed for the efficient control of graphics/video.

In regards to claims 3, 21: Gillespie et al in view of Surugucchi et al and Venkat teach the bridge attached to a AGP bus described above. Gillespie et al in view of Surugucchi et al and Venkat do not teach a north bridge. Applicants admitted prior art teaches a north bridge attaches an AGP bus. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use the bridge of Gillespie et al in view of Surugucchi et al and Venkat in the system of Applicants admitted prior art because this would have separated the graphics from the PCI system thus freeing the PCI system.

5. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prabhu et al PN 6,675,292.

In regards to claim 28: Prabhu et al teaches forming (configuring) a configurable register (Column 5 lines 41-56) that includes register configuration logic (the register is configurable, whatever allows/does the configuration is the configuration logic) and at least one register flop to contain an initial value (inherent the register is configured as read only if it had no initial value then the only possible value would be 0000.) and at least one mask flop (indication of read only or read write) that generates a mask bit for the configuration logic and wherein the register configuration logic configures the at least one register flop to be read only or read writable based upon the at least one mask value. Prabhu et al does not expressly teach the initial value and whether it is to be read only or read writable being stored in a memory only the configuring the

register as read only. Official notice is taken that configuration memory is well known. It would have been obvious to a person of ordinary skill in the art at the time of the invention to store the configuration info in a memory because this would have given it some place to come from.

6. Claims 10-11, 13, 15-17, 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie et al PN 5,859,987 in view of Surugucchi et al PN 6,094,699 and Venkat PN 5,857,083 as applied to claim 1 above, and further in view of Prabhu et al PN 6,675,292.

In regards to claims 10-11, 34-35: Gillespie et al in view of Surugucchi et al and Venkat teaches the configurable bridge as described above including the configuration registers. Gillespie however does not expressly state the configuration registers are themselves configurable. Prabhu teaches configurable registers as described above. It would have been obvious to a person of ordinary skill in the art to make the registers themselves configurable because this would have provided for greater configuration control.

In regards to claims 13, 16: Gillespie et al teaches multiple base address registers in accordance with the PCI specification incorporated by reference in Gillespie et al. The PCI specification notes the number of Base address registers in a bus bridge is 6.

In regards to claim 15: Gillespie et al teaches multiple base address registers in accordance with the PCI specification which teaches the base address registers having prefetchable and non-prefetchable and I/O space and non I/O space determinations. PCI spécification page 196.

In regards to claim 17: Gillespie et al teaches a configuration EEPROM. Which is an electrically erasable programmable ROM.

7. Claims 14, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie et al PN 5,859,987 in view of Surugucchi et al PN 6,094,699, Venkat PN 5,857,083 and Prabhu et al PN 6,675,292 as applied to claim 10 above, and further in view of Applicants admitted prior art.

In regards to claims 14 and 18: Gillespie et al does not teach the ASICs being graphics processors. Applicants admitted prior art teaches graphics processors (1020) attaches to a bus. It would have been obvious to include graphics processors because this would have allowed for the efficient control of graphics/video.

In regards to claim 12: Gillespie et al in view of Surugucchi et al and Venkat teach the bridge attached to a AGP bus described above. Gillespie et al in view of Surugucchi et al and Venkat do not teach a north bridge. Applicants admitted prior art teaches a north bridge attaches an AGP bus. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use the bridge of Gillespie et al in view of Surugucchi et al and Venkat in the system of Applicants admitted prior art because this would have separated the graphics from the PCI system thus freeing the PCI system.

Allowable Subject Matter

8. Claims 29-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In regards to claims 29-31: The examiner was unable to find the exact structure claimed.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul R. Myers

PRM
July 19, 2007